REPORT ON

SSCAS ARGENTINE SCHOOL OF MICRO-NANOELECTRONICS, TECHNOLOGY & APPLICATIONS

EAMTA · 2017

SAN MARTIN, BUENOS AIRES, ARG | JULY 22-29, 2017

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1. INTRODUCTION

The **Seasonal School on Circuits And Systemas** (SSCASS) Argentine School of Micro and Nanoelectronics, Technology and Applications (EAMTA) is a week-long school where undergraduate, graduate, master and Phd. students and professionals attend to intensive microelectronics courses, with the aim of promoting the development of related technology in the country and region. Its associated conference, CAMTA has become a technical forum of high technical quality for the meeting of researchers, technologists, and companies in the field of microelectronics.

The general objective of the school is to establish the development of advanced technology in the country, through the design of integrated circuits and their supporting technologies, maintaining a cohesion and periodic contact between the research and development groups in this area, forming and specializing advanced students through specific and intensive courses, involving the consuming and producing companies of technology, favoring the transfer of technology to the productive medium enterprises, and generating an environment for new activities, projects of collaboration and cooperation between members of the academy, companies, and abroad.

The school also includes an "Industry Day", where it favors the link with companies related to the area of microelectronics.

Between July 22 and 29, 2017, the twelfth Argentine School of Micro and Nano Technology and Applications (EAMTA) was held at the Miguelete Campus of the National University of San Martín (UNSAM), General San Martín, province of Buenos Aires, organized by School of Science and Technology (ECyT).

During the school, several courses of different level were dictated in parallel. Both basic and advanced courses were offered, in which the students are introduced to the design of integrated circuits (IC), as well as advanced, to perfect techniques of analog and digital design. Design courses, manufacturing and testing of IC technologies, and technologies associated with micro and nano electronics were also offered.

The Technical Program is also very diverse and rich. During the event, several lectures will be delivered by experts from Argentina, Brazil, Uruguay, Chile and Belgium. Industry day will count with known Semiconductor, Design and EDA companies from around the world, plus representatives of investment funds and important national electronic companies. This year, a work session with EDA and local companies will be held with the objective of setting up new initiatives to leverage local industry using new technologies.

One of the targets of the event is to help establish a technological platform in the country, and in doing this, we continue emphasizing the central role of students. Therefore, continuing with the tradition started in the first EAMTA, a record number of 107 grants (51 full lodging grants and 56 full travel grants) were provided to students from different provinces of Argentina, Chile and Uruguay. We want to thank all sponsors for making this possible. One hundred thirty (130) participants have registered for the event so far.

2. THE VENUE

Universidad Nacional de San Martín is an Argentinian State University, created in 1992 and has become a privileged space and a **leader in academic training, research, cultural development and social transformation**. It has a student population of around 20,000 students and an academic body of around 600 teachers and researchers.
It is located in General San Martin city, more commonly known as San Martín. This city has more than 420.000 inhabitants, and limits to the southeast with Buenos Aires City, being located 20km from BA's

center by car. Together with the National Institute of Industrial Technology (INTI), the Constituyentes Atomic Center (CAC-CNEA), the Institute for Scientific and Technical Research for Defense (CITEFA), the National Institute of Agricultural Technology (INTA), the Argentine Geological Institute (SEGEMAR), University of San Martín integrates the **Constituyentes Technological Pole** (PTC), which is an interface organization that allows the development of R&D projects and through exchange activities with other poles and technology parks.

The University is ranked as the number 12 in knowledge production in Argentina according to Scimago Ranking, and holds the second position in Argentina in terms of most publications in the best scientific journals of the world. This is the result of a distinctive combination of a socially engaged community, innovative programmes, and our great effort to pursue our mission, which is to support and develop **"the power of talent"**.

We developed strong, **research-led partnerships** with a range of leading universities in the world, especially in Europe and North America, such as École des Hautes Études en Sciences Socials, University of Paris 3-Sorbonne and Paris 8 (France), University of Kassel (Germany), University of Leeds (United Kingdom), Roma Tre University, Padova University (Italy), The New School University (Unites States), Karlsruhe Institute of Technology, among others.
The University's strongest fields of teaching and research are:

- **Science and Technology**, with many Engineering Degrees (Biotechnology, Telecommunications, Electronic, Vaccine, Environmental Studies, Nanoclays, Energy efficiency, Radionuclide, Transportation, Technology on Detection and Astroparticles, Medical Imaging, Diagnostic Imaging, Electromedicine, Computer Networking, Computer Programming, Laboratory, Nuclear Applications, Remote Sensing and Eco-IT)
- **Medical Sciences** (Rehabilitation science and technology, Biomedical applications, postgraduate medical programs)
- **Humanities and Social Sciences** (Political Science, Anthropology, Sociology, History, Philosophy, Local Development, Economics and Management, Psycopedagogy and Education, Chinese and Slavonic Studies)
- **Arts** (Cultural Heritage Research, Restoration, Object and Puppet Theatre, Dance, Combined Performing Arts, Documentary Film)

The UNSAM has signed almost **400 international agreements**, from which have emerged or consolidated projects of investigation and various programs in: students and teachers exchange, joint cathedras, joint degrees and fellowships.

The University is constantly open for new partnerships based on academic and student exchanges, teaching, joint research, special programmes and innovation with leading universities and institutions.

3. TRACKS/COURSES

This year, six courses were offered during EAMTA. The basic track (30 attendees) covers basic topics on analog circuits, digital circuits, tools, device physics and design laboratories with EDA tools. An additional analog course provides hands-on design of CMOS amplifiers (21 attendees). Synopsys delivers a track covering advanced digital techniques (19 attendees) and entry-level knowledge of digital design flow and advanced industrial tools & techniques for digital synthesis. A microfabrication track provided a general insight to deposition techniques related with micro-devices fabrication, as well as pre-deposition strategies and post-deposition alternatives (15 attendees). In addition, a

specialized track in design and test of fault-tolerant embedded systems for aerospace applications (29 attendees) and a basic digital track based on FPGA (11 attendees) were dictated.

3.1 Basic VLSI design

30 attendees

3.1.1 Goal

Provide the student knowledge of the physical fundamentals of the operation of MOS devices, as well as the principles fundamentals of the CMOS microfabrication process. Also, let the student acquire the ability to design basic analog and digital circuits, as well as the use of CAD tools.

3.1.2 Teaching Team

- ***VLSI Introduction***
  Dr. Pedro Julián (UNS, Bahía Blanca)
- ***MOS Devices Physics***
  Dr. Adrián Faigón (FIUBA, Buenos Aires)
- ***Introduction to analog design***
  Dr. Luis Toledo (UCC, Córdoba)
- ***Project***
  Ing. Fabricio Alcalde Bessia (IB)
  Ing. Sebastián Pazos (UTN.FRBA)
  Ing. Gabriel A. Sanca (ECyT.UNSAM)

3.1.3 Hands-on Project: 4-bits counter

Let the student know the physical fundamentals of the operation of MOS devices, as well as the fundamental principles of the manufacture of CMOS integrated circuits. Also, let the student acquire the ability to design basic analog and digital circuits, as well as the use of CAD tools.

- The objective of this activity is to propose a moderate design problem to test the use of the VLSI circuit design tools provided by Synopsys Inc.
- The student will have to verify logic and electrically the circuit that is presented, and once passed this stage, proceed to design the circuit's physical layout.

3.2 Analog design

21 attendees

3.2.1 *Goal*

The goal of this course is to provide basic theoretical and practical tools for the design of analog circuits over integrated circuits (chips). The design techniques analyzed in the course provide a basis for the design of amplifiers in CMOS processes. Laboratory practices will emphasize high-speed operational amplifiers.

3.2.2 Minimum Content

- **Review of MOS structure and circuit modeling:**
  Physics of the semiconductor metal-oxide transistor (MOS). MOS transfer I/V. Second order

effects. MOS model: parasitic capacitors, small signal model, physical device design. Long channel vs short channel models.

- **Single stage amplifiers:**
  Common source, source follower and common gate configurations. Cascode stage.
- **Differential amplifiers**:
  Topologies. Common mode response. Differential pair with resistive load and MOS load.
- **Power Mirrors and Active Loads:**
  Passive current mirror and cascode. Analysis in large signal and small signal.

3.2.3 Teaching Team

- Dr. Ing. Benjamín Reyes (UNC-CONICET)
- Ing. Ronald Valenzuela (Synopsys Inc., Chile)
- Ing. Laura María Biolato (UTN-FRC)

3.2.4 Hands-on Project: Op. Amp.

Design and characterization of a Miller type operational amplifier based on specifications: Linearity, bandwidth, slew rate, maximum swing. Simulation conditions: process, voltage and temperature variations (PVT conditions).

3.3 Basic digital design

11 attendees

3.3.1 Goal and abstract

The course aims to teach the basics of digital design.

In the first part it is reviewed the concepts of the HDL Verilog language and it is presented the basic elements of the digital design: Combinational circuits and sequential circuits.

During the second part the concepts of time and the delays of the gates and signals are addressed, in order to understand how to properly design a digital circuit. It is shown the importance of correct design, not only from the logical point of view, but also from the time domain, this is to make it work efficiently or, in our case, fast enough to meet the application requirments.

In the third part, a synchronous circuit will be simulated and implemented in an FPGA. During this process it will be verified that all the constraints are met and finally its logical operation will be validated.

Minimum Content

- Introduction to Verilog.
- Combinational, sequential and complexes circuits.
- Binary representation, fixed point and floating point.
- Temporal diagrams of combinational and sequential circuits.
- Examples combining basic elements to form other complex elements.
- Timing of the circuits.
- Synchronous circuits and delay of the gates.

- Characteristic times of the FF.
- Implementation of basic circuits in FPGA.

Teaching Team

- Dr. Ing. Ariel L. Pola (Clariphy-Fundación Fulgor)
- Ing. Nicolás Álvarez (UNSAM-FIUBA)
- Ing. Federico Zacchigna (FIUBA)

3.4 Advanced digital design

19 attendees

3.4.1 Goal

To give the student the knowledge about the problems and tools related to the design of specific application integrated circuits (ASIC), including problems related to time, performance and power optimization, and verification tests.

Let the student understand the theory and tools involved in designing large-scale digital integration systems (VLSIs) for architectures with millions of transistors.

That the student learn to use the Hardware Language for the design of digital systems.
That the student understands the different Design metrics: number of devices and area of implementation, switching speed, energy dissipation and power.

3.4.2 Minimum Content

- Introduction to the digital world and ASIC design flow
- Design of digital systems using VerilogHDL
- Finite State Machines
- Time Related Design
- Hierarchy and Partitioning
- Low Power Design
- Test, simulation and testbench design

3.4.3 Teaching Team

- Ing. Victor Grimblatt (Synopsys Inc., Chile)
- Ing. Esteban Viveros (Synopsys Inc., Chile
- Ing. Gonzalo Fernandez (Synopsys Inc., Chile)

3.5 Microfabrication and testing techniques

15 attendees

3.5.1 Goals

Provide a general insight to deposition techniques related with microdevices fabrication, as well as pre-deposition strategies (surface preparation, buffer materials) and post-deposition alternatives (to modify and/or improve some aspects).

Offer a full perspective about testing techniques regarding functionality.

Ensure a deep comprehension about clean-room features (deposition techniques, substrate quality, materials impurity content) and their impact on devices' performance.

3.5.2 Minimum Content

- **Introduction to Cleanroom environment**
- **Substrate reparation:** Introduction, substrates types and cleanning
  Chapters of Fransilla: 1, 4, 12 and 13
- **Lythography**
  Chapters of Fransilla: 8, 9 and 10
- **Deposition techniques**
  Chapters of Fransilla: 5, 6 and 7 and sputtering in detail
- **Electrical characterization**
  Chapter of Schroder: 1 and general remarks of experimental setup to be used
- **Etching techniques**
  Chapters of Fransilla: 4, 20 and 21
- **Structural characterizaction**
  Chapters of Fransilla: 2, Chapter of Ohring: 2
- **LOCOS process**

3.5.3 Teaching Team

- Dr. Ing. Federico Golmar (UNSAM-CONICET)
- Dr. Cynthia Quinteros (CAB.CNEA-CONICET)
- Lic. Mariano Barella (UNSAM-CONICET)

3.6 Design & Test of Fault-Tolerant Embedded Systems for Aerospace Applications

29 attendees

3.6.1 Goal

- Let the student understands methodologies of design of systems fault-tolerant, redundancy by hardware and software, based on information and time.
- Let the student understands physical mechanisms that cause errors or affect the reliability in environments with ionizing radiation.
- Let the student understands methodologies of system testing.

3.6.2 Minimum Content

0) Introduction to CMOS technologies
0.1) CMOS circuits and MOS transistors
0.2) Bulk vs SOI CMOS technologies, FINFETs
1) Fault-Tolerant (FT) Systems: Basic Concepts
1.0) Space environments
1.1) Total-Ionizing Dose (TID)
1.2) Single-Event Effects: Single-Event Upset (SEU), Single-Event Transient (SET)

1.2.1) Electrical model for SEU simulation in SPICE
1.3) Electromagnetic Interference (EMI)
1.4) Test environment and standards for electronics qualification
2) Hardware Redundancy
2.1) Passive
2.2) Active
2.3) Hybrid
3) Software Redundancy
3.1) Error Detecting and Correcting Codes – EDAC
3.1.1) Parity
3.1.2) Berger
3.1.3) Arithmetic
3.1.4) Checksum
3.1.5) CRC
3.1.6) Hamming
3.1.7) Examples
4) Information Redundancy
4.1) Consistency and Capacity Checks
4.2) N-Programming Version
4.3) Recovery Blocks
5) Time Redundancy
5.1) Detection of Transient and Permanent faults
5.2) Detection and Correction of Permanent Faults
6) Aging of Electronics
6.1) Definition, detection and recovery from aging
6.2) On-chip aging sensors
7) Reliability and physics of failure
7.1) Introduction and basic definitions
7.1) Vulnerabilities originating in die
7.2) Vulnerabilities arising from bonding
7.3) Vulnerabilities originated in the encapsulation
7.4) Vulnerabilities and failures in the life-cycle context of integrated circuits

3.6.3 Teaching Team

- Dr. Fabian Vargas (PUCRS)
- Dr. Ing. José Lipovetzky (IB-CAB.CNEA)
- Ing. Roberto Manuel Cibils (INVAP SE)
- Dr. Ing. Mariano García Inza (FIUBA-CONICET)

4. LECTURERS

EAMTA 2017 speakers

As traditionally, plenary talks are held on Mondays, Tuesdays and Wednesdays at EAMTA. Here, we present this year speakers and talks:

Intelligent Materials: the new frontier of nanotechnology

Dr. Galo Soler Illia *(INS, UNSAM)*

Abstract. Materials exhibit an unusual behavior when their size is on the nanometer scale, due to changes in their electronic structure, the huge surface-volume relationship and the confinement of matter. At the nanoscale the quantum behavior of matter and its molecular nature are revealed. Today a huge variety of nanomaterials with custom properties is known, which is possible to produce from the techniques of molecular chemistry, supramolecular and materials. In this talk, I will show examples of how complex nanosystems, composed of several different types of nanomaterials, can be designed from building blocks and assembly principles using nanoscale forces. These nanosystems are capable of generating signals or responding to external stimuli, and can also integrate and connect to the most common platforms of optics and electronics, opening the possibilities to new intelligent devices.

Day: *Monday, July 24*

EUV lithography: what it takes to keep on shrinking

Dr. Ing. Nicolás Nemirovsky *(ITBA)*

Abstract. Moore's Law tells us that the number of transistors in an integrated circuit doubles every two years. It is used by consumers as an indication on how much smaller, faster, better electronics will be in the future. However, in the semiconductor industry, Moore's Law is what sets the industry a target, what drives it.

In the heart of miniaturization lies lithography, since it drives some key parameters: imaging, which indicates how small a feature can be created, and overlay, which says how well can two layers of features be positioned with respect to one another.

Today, each nanometer increase in resolution and precision is only possible with significant efforts from multidisciplinary teams, and an ever-increasing investment in R&D. This can be clearly seen in Extreme UltraViolet (EUV) lithography technology, which is enabling the next semiconductor nodes, effectively prolonging Moore's laws for the coming years.

These machines create EUV light by bombarding tiny droplets of tin with a high-power infrared laser with enough power to create a tin-plasma bubble, within an ultra-clean high vacuum consisting of an extremely low pressure of hydrogen. Many aspects of this technology are, in themselves, a technological breakthrough: from being able to create dozens of thousands of micrometer-wide tin droplets in one second, to being able to focus, fire and hit those droplets twice, in mid-flight, with one of the most power lasers in the world. This is an exemplary case-study where science and technology meet engineering to deliver the next step in semiconductor manufacturing.

Day: *Tuesday, July 25*

Smartness Is Everything – From Silicon to Software

Ing. Victor Grimblatt *(Synopsys, Inc.)*

Abstract. Last year, in Seoul, a computer program called AlphaGo defeated 9 dan, and 18 times Go world champion Lee Se-dol by a score of 4-1. This year, in Barcelona, SoftBank Founder & CEO, Masayashi Son, in his MWC17 keynote predicted that by 2045 computers made with chips integrating 3 quadrillion transistors, will have a 10,000 IQ. Artificial intelligence is changing the rules of the game: new computing architectures are emerging that lead to new classes of processors in the cloud, as well as in the "things" aimed at revolutionizing our life: robotics, cars, homes, phones, "every thing" gets smarter. It is hard to overstate the promises and the challenges we are facing in the new applications emerging in the age of smarter "every thing".

Moore's law continues, quasi-relentlessly to enable exponentially larger chips manufactured using Angstrom-level process technologies, thus requiring smarter IC design tools; artificial intelligence may have an impact also on EDA, where the sheer complexity, which is approaching the limits of "plain"

computation, could be addressed by “teaching” a “brain” how to solve certain classes of problems. Beyond Moore, better, tighter, smarter “integration” of processors and memory, delivering much higher bandwidth, enables new classes of processors – such as TPU – exponentially more parallel in architecture, thus enabling faster “machine learning”. On the one hand, AI may help EDA leapfrog the sheer complexity of Angstrom-level process technologies; on the other hand, innovative EDA may help AI happen.

Our entire industry is under pressure to de-risk and speed-up the critical intersections. Smartness is “every thing”!

Day: *Wednesday, July 26*